

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-6, 8, and newly submitted Claims 19-21 are presently active in this case. Claims 9 and 11 having been withdrawn from consideration is directed to a non-elected invention, Claims 7 and 12-18 having previously been canceled, and Claims 1 and 8 having been amended by the present amendment.

In the outstanding Office Action, Claims 1, 4, 6 and 10 were rejected under 35 U.S.C. § 103 as being unpatentable over Schutten et al. (4,541,001) in view of Buluchea et al. (5,072,266); and Claims 2 and 3 were rejected under 35 U.S.C. § 103 as being unpatentable over Schutten in view of Buluchea, and further in view of Schieh et al. (5,929,481).

In light of the outstanding grounds for rejection, Claim 1 has been amended to clarify the claimed invention and thereby more clearly patentably define over the applied prior art. To that end, amended Claim 1 further defines the claimed semiconductor device as including a boundary portion between the first semiconductor region and the second semiconductor region and a portion of the trench crossover each other. With such structure, the semiconductor device of amended Claim 1 is designed to minimize an overlapping area between gates (first and second gate electrodes) and a drain (first semiconductor region) such that the capacity between the gates and the drain is decreased.

Also submitted herewith are new Claims 19-21. Claim 19 is dependent upon Claim 8 and recites the above-noted additional features added to Claim 1. New Claims 20 and 21 recite that “a deepest portion of the second semiconductor region has an impurity concentration not higher than an impurity concentration of a channel region of the second semiconductor region formed along side surfaces of a trench in which the first and second

semiconductor electrodes are formed.” The features stated in Claims 20 and 21 are consistent with Applicants’ disclosure in which the deepest portion of the second semiconductor region (p-type base region 13) is a region which gradually mixes with the first semiconductor region (n-type epitaxial layer 12) due to the manufacturing process, and has a concentration substantially not higher than the concentration of the channel region. Accordingly, no new matter has been added by the present amendment.

Turning now to the outstanding grounds for rejection of Claim 1, as above-noted, the semiconductor device recited in amended Claim 1 has a structure in which “a boundary portion between the first semiconductor region and the second semiconductor region and a bottom portion of the trench cross each other.” With such structure, the semiconductor device recited in amended Claim 1 is designed to minimize the overlapping area between the gates and the drain, such that the capacitance between the gates and the drain is decreased.

Schutten et al. describes a power FET in which a notch 12a (12) is formed in a substrate 4a (4) and p regions 54a (54) and 56a (56). On both sides of the notch 12a, gate electrodes 34a (34) and 36a (36) are formed via silicon dioxide insulating layers 30 and 32. The gate electrodes 34a and 36a are formed separately from each other (see FIG. 7 (1) and the like).

Bulucea et al. describes “a central portion 27c of the body region lies below a plane that is defined by the bottom of the trench 29 for the transistor cell” (See Fig. 8, column 6, lines 27-61).

The outstanding Office Action acknowledges that Schutten et al. does not describe that a depth of the trench is shorter than a depth of a deepest bottom portion of the second semiconductor region. The outstanding Office Action relies on Bulucea et al. as disclosing that structure.

In light of such analysis in the outstanding Office Action, amended Claim 1 clarifies further that “a boundary portion between the first semiconductor region and the second semiconductor region and a bottom portion of the trench cross each other.”

Schutten et al. teaches, as shown in FIG. 7 (1), that a boundary portion between a substrate 4a (4) and a p region 54a (54) and a side portion of a notch 12a (12) cross each other. Schutten et al. does not teach or suggest, however, that the boundary portion between the substrate 4a (4) and the p region 54a (54) and a bottom portion of the notch 12a (12) cross each other.

Bulucea et al. teaches, as shown in FIG. 8 and the like, that a boundary portion between an epitaxial layer 25 and a body region 27 and a side portion of a trench 29 cross each other. Bulucea et al. does not teach or suggest, however, that the boundary portion between the epitaxial layer 25 and the body region 27 and a bottom portion of the trench 29 cross each other.

As stated above, Schutten et al. discloses a structure in which gate electrodes are separated from each other in a trench. Bulucea et al. (and Hshieh et al.) discloses a structure in which a deepest portion of a body region has a greater depth than a bottom portion of a trench. Schutten et al. and Bulucea et al. do not disclose, however, a structure for minimizing the overlapping area between the gates and the drain for the purpose of decreasing the capacitance between the gates and the drain, that is, a structure recited in amended Claim 1 in which “a boundary portion between the first semiconductor region and the second semiconductor region and a bottom portion of the trench cross each other.” Hence, it is respectfully submitted that the structure recited in amended Claim 1 is patentably distinguishing over the combined teachings of Schutten et al. and Bulucea et al. Therefore,

the rejection of Claim 1 under 35 U.S.C. 103(a) as being unpatentable over Schutten et al. in view of Bulucea et al. has been overcome.

Similarly, Claims 2-4, 6 and 10 depend on amended Claim 1, the grounds for rejection of Claims 2-4, 6 and 10 under 35 U.S.C. 103(a) are also overcome by virtue of the noted dependency.

New Claims 20 and 21 define a structure in which “a deepest portion of the second semiconductor region has an impurity concentration not higher than an impurity concentration of a channel region of the second semiconductor region formed along side surfaces of a trench on which the first and second gate electrodes are formed.”

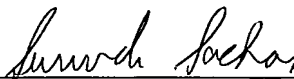
On the other hand, a body region described in each of Bulucea et al. and Hshieh et al. has a structure in which a deepest portion deeper than a bottom portion of a trench has an impurity concentration of p+, which is higher than an impurity concentration of any other portions of the body region. Hence, the above-described structure recited in new Claims 20 and 21 is not disclosed in Bulucea et al. and Hshieh et al.

In amended Claim 8, the limitation “the trench having no second semiconductor region under its bottom surface” has been deleted. Applicants consider this to be an unnecessary limitation to distinguish patentability over the cited references. Accordingly, even without the limitation, amended Claim 8 has advantages distinguished over the references. Applicants therefore consider that amended Claim 8 should be allowed despite deletion of the above-mentioned limitation.

Consequently, in view of the present amendment, and in light of the above discussion, the pending claims as amended herewith are believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number

22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 03/06)

Surinder Sachar
Registration No. 34,423